INTEGRATED CIRCUIT MEMORY DEVICES HAVING ZIG-ZAG ARRANGEMENTS OF COLUMN SELECT IO BLOCKS TO INCREASE INPUT/OUTPUT LINE ROUTING EFFICIENCY

Abstract of the Disclosure

Integrated circuit memory devices include sense amplifier arrays having layouts that are configured to support greater pitch between adjacent input/output lines, while maintaining high levels of integration density. A sense amplifier array is provided having first and second column select I/O blocks that are arranged in an alternating zig-zag layout sequence, with the first column select I/O blocks positioned in a first row of the sense amplifier array and the second column select I/O blocks positioned in a second row of the sense amplifier array. The sense amplifier array also includes an alternating zig-zag layout sequence of first and second N-type (or P-type) sense amplifier blocks that extends back-and-forth between the first and second rows. The zig-zag layout sequence of sense amplifier blocks is interleaved with the zig-zag layout sequence of the column select I/O blocks.

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